SC12161ET

Claims

1.   A continuous time sigma delta converter comprising:
conversion means (510, 520, 530, 540, 560) having known non-ideal characteristics

5   and arranged to provide an output signal;
a compensation circuit (570) comprising error modelling components (370, 375, 380, 385, 390, 395) arranged to substantially model the non-ideal characteristics of the conversion means (510, 520, 530, 540, 560); and
summation means (490) coupled to combine the compensation signal with the output

10   signal in order to provide a compensated output signal.

2.   The converter of claim 1 further characterised by: the summation means (580) being arranged to subtract the compensation signal from the output signal in order to provide the compensated output signal.

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3.   A compensation circuit (570) for use with a continuous time sigma delta converter (510, 530, 540, 560) having known non-ideal characteristics, the compensation circuit (570) comprising error modelling components (370, 375, 380, 385, 390, 395) arranged to substantially model the non-ideal characteristics of the

20   converter 510, 530, 540, 560) in order to provide a compensation signal,
wherein the compensation signal is combinable (580) with a non-ideal output of the converter (510, 530, 540, 560) in order to provide a compensated output signal.

4.   A method for compensating for known non-ideal characteristics in a

25   continuous time sigma delta converter (510, 530, 540, 560), the method comprising:
converting an input signal of one time domain to an output signal of another time domain using a converter (510, 530, 540, 560) having known non-ideal characteristics;
modelling the non-ideal characteristics of the converter in a compensation circuit

30   (570);

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combining a compensation signal output of the compensation circuit (570) with the output signal of the converter (510, 530, 540, 560) in order to provide a compensated output signal.

5   5.   The converter of claim 1 or claim 2, circuit of claim 3 or method of claim 4 further characterised by: the non-ideal characteristics being associated with a feedback path (540) of the converter.

6.   The converter, circuit or method of any preceding claim further characterised
10   by: the non-ideal characteristics including symmetrical errors (235) associated with non-ideal rising and falling edges (230) of signal transitions of the converter (510, 530, 540, 560).

7.   The converter, circuit or method of any preceding claim further characterised
15   by: the non-ideal characteristics including asymmetrical (245) errors associated with non-ideal rising and falling edges (230) of signal transitions of the converter (510, 530, 540, 560).

8.   The converter, circuit or method of any preceding claim further characterised
20   by: the compensation circuit (570) having calibration parameters (375, 395) determined by an dichotomy technique which iteratively refines the values of the calibration parameters (375, 395).

9.   A method for producing calibration parameters for use in the compensation
25   circuit (570) of any preceding claim, the method comprising the steps of:
collecting output samples from the converter (510, 530, 540, 560);
calculating a Signal to Noise and Distortion Ratio of the collected data;
determining whether the calculated Signal to Noise and Distortion Ratio meets specified performance criteria;
30   selectively recalculating the Signal to Noise and Distortion Ratio in dependence upon the step of determining, using a calibration algorithm (600-695).

10.   The method of claim 9 wherein the calibration algorithm uses a dichotomy technique (600-695) which iteratively refines the values of the calibration parameters.